

**Amendments to the Claims:**

This listing of the claims will replace all prior versions and listings of claims in the application:

**Listing of Claims:**

1. (Canceled)

2. (Amended): A nonvolatile semiconductor memory device comprising:

a main bit line formed of metal wiring;

first and second subbit lines connected in series, each formed of metal wiring and aligned parallel to said main bit line;

first and second switching transistors, each responsive to a sector select signal for connecting said main bit line to a corresponding one of said first and second subbit lines;

a first memory cell group including  $n$  memory cells ( $n \geq 2$ ), each connected to said first subbit line;

a second memory cell group including  $n$  memory cells, each connected to said second subbit line;

wherein

at least a part of the main bit line and at least a part of the subbit lines are formed in different layers,

each of said memory cells includes a control gate, a floating gate, a drain, and a source, and

each of said memory cells is connected to a corresponding one of said first and second subbit lines via said drain; said device further comprising

$n$  connection lines, each for connecting the control gate of a  $j$ -th memory cell ( $j=1, 2, \dots$ ,

n) in said first memory cell group located in a direction farther from said second memory cell group to the control gate of a j-th memory cell in said second memory cell group located in a direction farther from said first memory cell group; and

row decoder means responsive to an externally applied address signal for selecting one of said n connection lines.

3. A nonvolatile semiconductor memory device, comprising:

a main bit line formed of metal wiring;

first and second subbit lines connected in series, each formed of metal wiring and each aligned parallel to said main bit line;

first and second switching transistors, each for connecting said main bit line to a corresponding one of said first and second subbit lines;

a first memory cell group including n ( $n \geq 2$ ) memory cells, each connected to said first subbit line;

a second memory cell group including n memory cells, each connected to said second subbit line,

wherein

at least a part of the main bit line and at least a part of the subbit lines are formed in different layers,

each of said memory cells include a control gate, a floating gate, a drain and a source, and

each of said memory cells is connected to a corresponding one of said first and second subbit lines via said drain,

said device further comprising:

n connection lines, each for connecting the control gate of a relevant memory cell in said first memory cell group to the control gate of a corresponding memory cell in said second memory cell group; and

a row decoder, responsive to an externally applied address signal for selecting one of said n connection lines.

4. The nonvolatile semiconductor memory device according to claim 3, wherein said n connection lines are formed of polycrystalline silicon, and wiring for connection between said row decoder and said n connecting lines is formed of metal wiring.

5. A nonvolatile semiconductor memory device, comprising:

a first bit line formed of metal wiring;

a switch having a conductive end connected to said first bit line;

a second bit line formed of metal wiring connected to other conductive end of said switch;

a plurality of memory cells connected to said second bit line, each including a drain, a control gate, a floating gate and a source; and

a source line formed with an active layer, to which said sources of said memory cells are commonly connected,

wherein

at least a part of the first bit line and at least a part of the second bit line are formed in different layers.

6. A nonvolatile semiconductor memory device, comprising:

a first bit line formed of metal wiring;

a switch having a conductive end connected to said first bit line;

a second bit line formed of polycrystalline silicon connected to other conductive end of said switch;

a plurality of memory cells connected to said second bit line, each including a drain, a control gate, a floating gate and a source; and

a source line formed with an active layer, to which said sources of said memory cells are commonly connected.